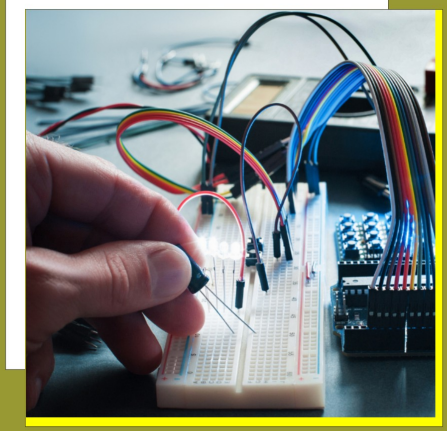
MICROPROCESSORS



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CONTENT

CHAPTER - 1

MICROPROCESSOR 8085

- A microprocessor unit is generally referred as MPU
- MPU is designed with ALU, control unit and some count of processing Registers and these registers are used to store the data temporarily during program execution
- Generally different MPUs available are specified like 8 bit, 16 bit, 32 bit and so on.
- Bit capacity of MPU is defined as the no.of bits it can process at a time in parallel .i.e. an 8 bit MPU can perform all 8 bit operations at a time
- In general, the internal architecture of the microprocessor depends on the bit capacity of the micro processor
- The system bus of MPU consist of 3 types of buses known as address bus ; data bus and control bus.
- Address signals are generated by MPU and sent to memory to identify the address of the memory through address bus and it is unidirectional bus.
- Data bus is used to transfer the data in between memory and MPU
- Control signals are generated by MPU and these signals are transferred in between memory and MPU and used to provide timing for various operations
- Control signals are used to perform the required operations.
- MPU can primarily perform 4 operations ; Memory Read ; Memory write ; I/O Read and I/O write; and for each operation it generates the appropriate control signals

8085 Microprocessor

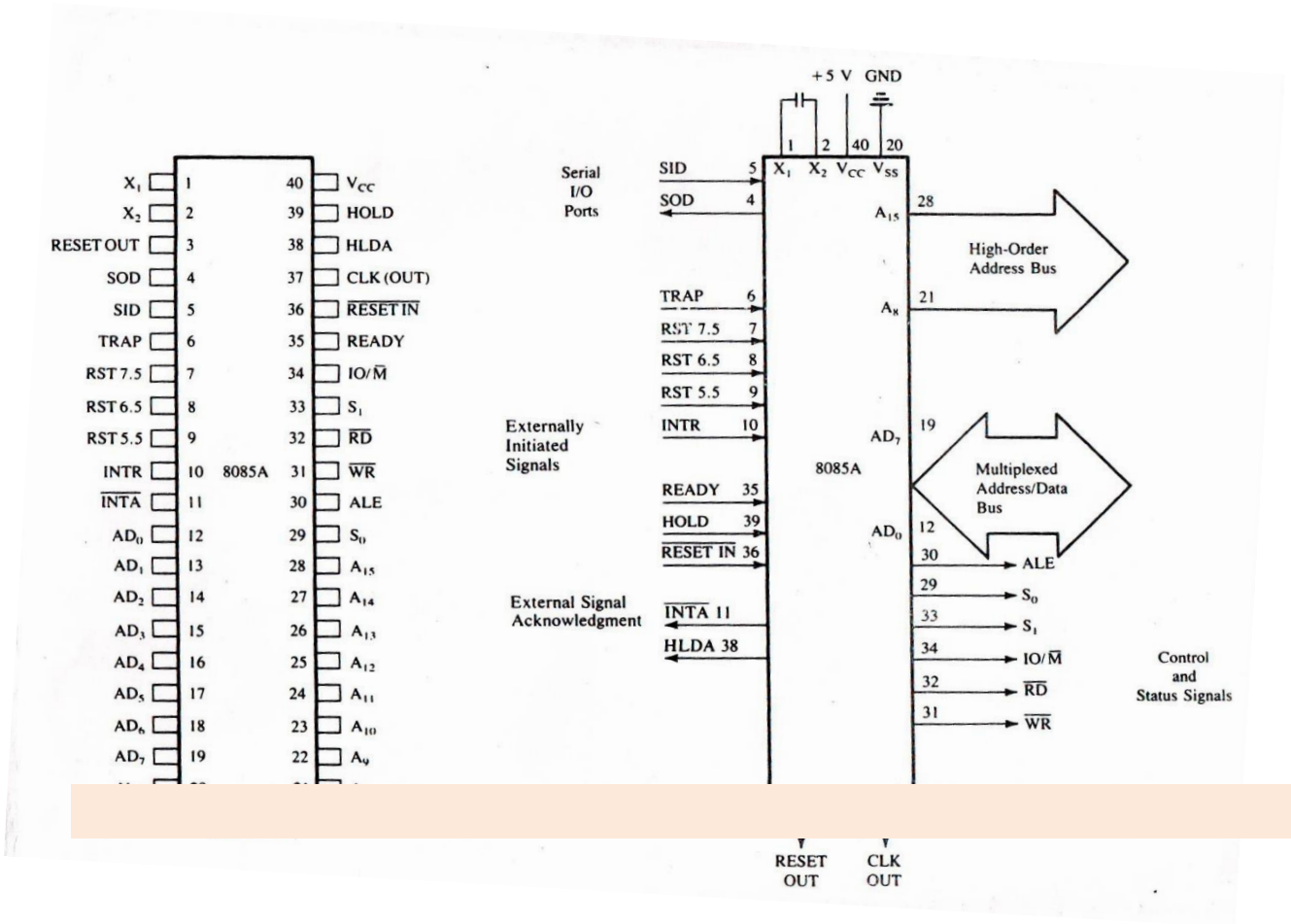
- It is a 40 pin I.C with operating voltage 5 volts
- It is designed with 2 MH and 3.07 MHz frequencies
- Max clock frequency of 8085 is 3.07 MHz (3MHZ)
- Crystal frequency is double to its clock
- 8085 MPU is designed with on chip clock generator i.e. no external oscillator is required

- 8085 MPU has 74 basic instructions and 246 opcodes
- 8085 supports 5 no.of hardware interrupts and 8 no.of software interrupts

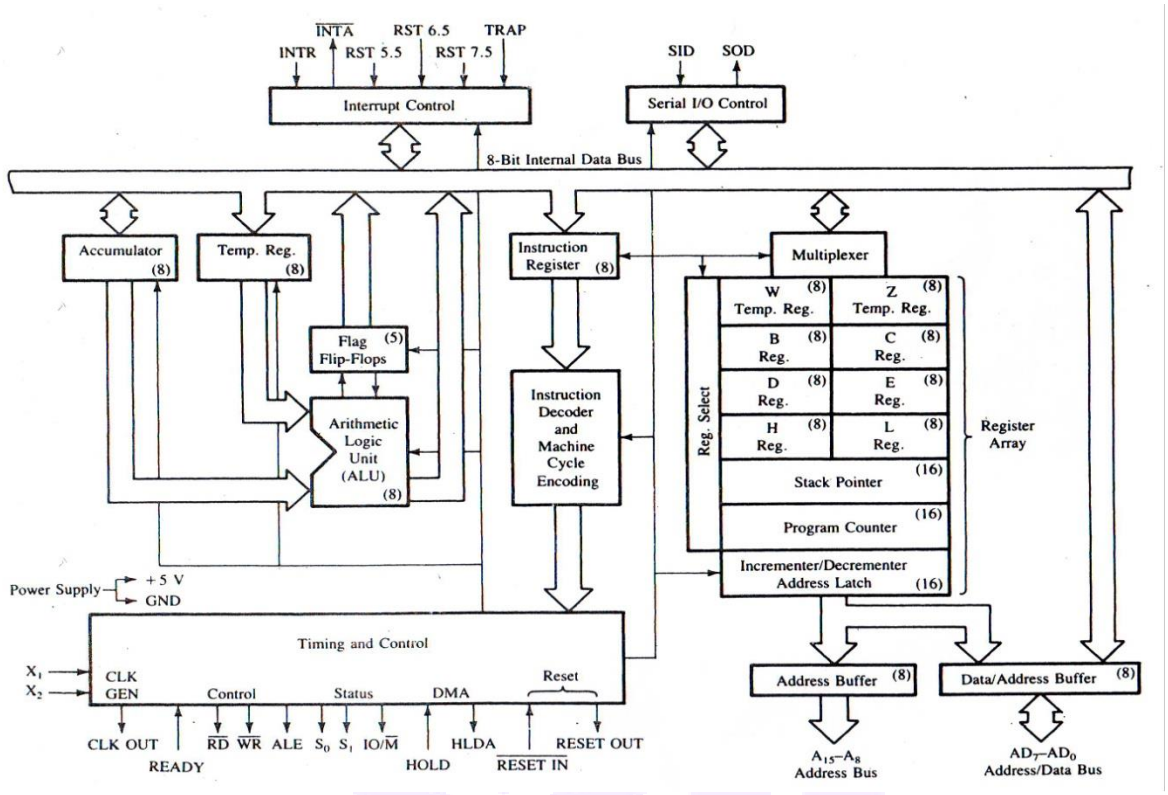
- Hardware interrupts are Trap ; RST 7.5; RST 6.5; RST 5.5 and INTR
- Trap has the highest priority among all
- But trap has lower priority than DMAC during DMA
- Trap is also known as RST 4.5
- INTR has the lowest priority
- No.of software interrupts for 8085 are 8, and range from RST '0' to RST '7'
- Opcode length varies from 1 byte to 3 byte
- Instructions, having the 16 bit address in the given instruction known as 3 byte instructions Ex : Call 2500H
- Instructions, having the 8 bit data or port address in the given instruction is 2 byte instruction Ex : MVI A, 35H
- Instruction with neither 16 bit address nor 8 bit data is known as 1 byte instruction Ex : MOV A, B
- In 8085 MPU ; 5 No.of flags are available and these flags are also known as status flags; known as carry (cy) ; Auxilary carry (Ac) ; Sign (s) ; parity (P) and zero (z)
- 8085 MPU has 2 no.of 16 bits Registers known as program counter (PC) and stack pointer (SP)
- PC always holds the address of the next instruction to be executed
- SP always holds the address of the top of the stack
- 8085 MPU has 8 bit accumulator and 8 bit flag Register ; and this combination is known as PSW (Program status word)
- 8085 MPU is designed with 6 no.of general purpose registers along with A and F ; these register are known as B, C ; D E and H, L.
- These 8 bit general purpose register can be used as 3 no.of 16 bit Register Pairs when required like BC, DE and HL pairs
- 8085 MPU has 16 no.of address lines and 8 no.of data lines
- Memory size of any MPU depends on the no.of address lines
- Total no.of Memory locations that can be accessed by 8085 MPU is 2^{16} =64 K = 65536
- In Hex code ; the memory ranges from 0000 H to FFFFH
- The lower 8 no.of address lines are multiplexed with 8 data lines and specified as AD_0 to AD_7
- Multiplexing of address and data lines is used to reduce the hardware size of MPU
- The no.of Machine clycles required to execute an 8085 MPU instruction varies from one of five

- Max no.of 'T' states for executing an instruction are 18 and minimum no.of 'T' states required for executing an instruction are 4
- Max no.of machine cycles required are 5 and minimum one
- 'T' state value depends on the clock frequency
- Group of 'T' states is known as machine cycle
- Group of machine cycles is known as execution cycle

Signal description of 8085 MPU



The 8085A Microprocessor Functional Diagram



- Total no.of signal pins (40) are divided in to 6 Groups
  1) Power supply and frequency
  2) serial I/O ports
  3) Address Bus
  4) Data bus
  5) Interrupts and externally initiated signals
  6) Status, control and Acknowledge signals
- SID and SOD signals are used for serial communication
- SIM and RIM instructions are used for serial I/O communication
- A.L.E. is used to generate the lower order address lines (A,→ A_0)
- S_1, S_0 and IO/$\overline{M}$ signals are called status signals
- $\overline{RD}$ and $\overline{WR}$ signals are control signals
- HOLD and HLDA are used for DMA operation
- READY signal is used by the MPU to communicate with slow operating peripherals

- $\overline{RESETIN}$ is active low signal to chip Reset
- RESET out signal is used to connect to RESETIN of other inter facing circuits used in microprocessor based system
- CLOCKOUT of 8085 will be connected to CLOCKIN of other interfacing ckts used in microprocessor based system to synchronize the operation with 8085
- So and S_1 signals are used to indicate the current status of the processor

S_1	S_0	Status
0	0	Halt
0	1	Write
1	0	Read
1	1	Fetch

- The process of getting / reading the opcode from memory to C.P.U is known as opcode fetch
- The process of getting / reading the data from memory is known as operand fetch
- By combining the status signals IO/ $\overline{M}$ with control signals $\overline{RD}$ and $\overline{WR}$ we can generate the following operations, $\overline{MEMR}$, $\overline{MEMW}$, $\overline{IOR}$ and $\overline{IOW}$

IO/ $\overline{M}$	$\overline{RD}$	$\overline{WR}$	Operation
0	0	1	Memory Read
0	1	0	Memory write
1	0	1	I/O Read
1	1	0	I/O Write

- All software interrupts are vectored interrupts
- Hardware interrupts are of 2 types a) vectored interrupts b) Non – vectored interrupts
- RST 7.5, RST 6.5, RST 5.5, and RST 4.5 are called Hardware vectored interrupts
- INTR is called Hardware non vectored interrupt
- Interrupts vectored address

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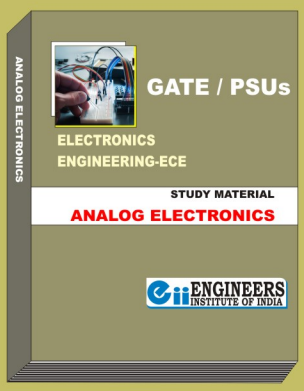

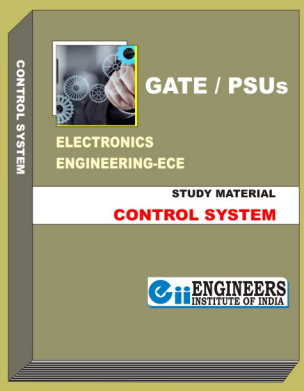

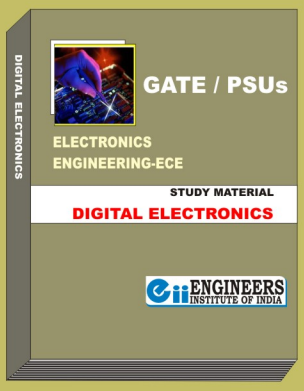

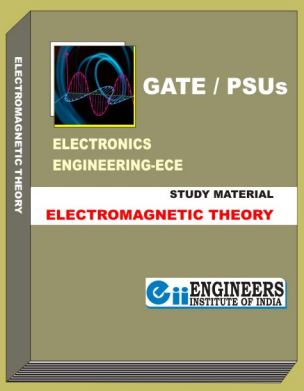

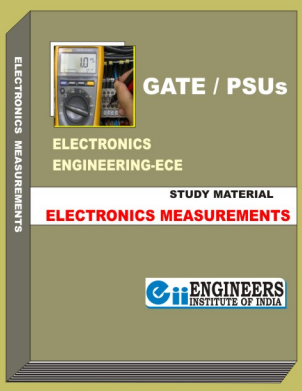

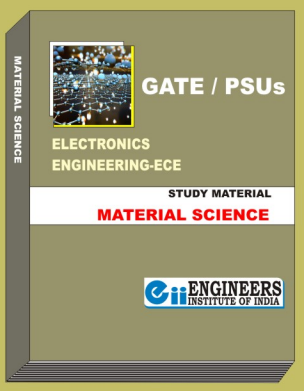

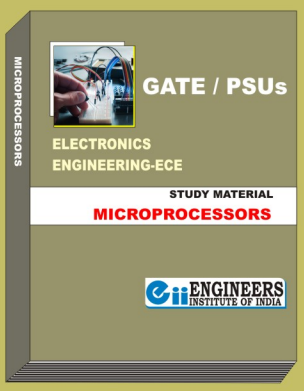

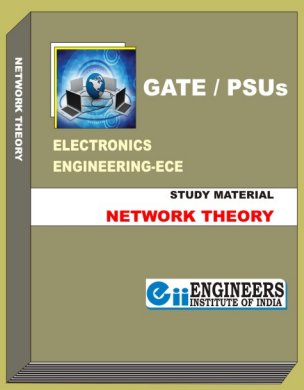

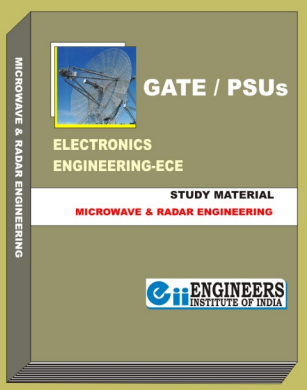

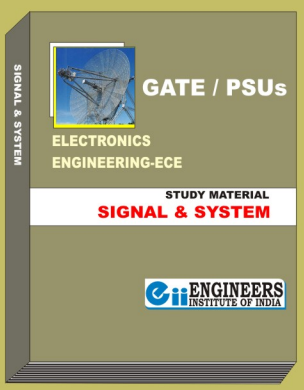

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